

K4S64323LF-S(D)G/S

CMOS SDRAM

**2Mx32
Mobile SDRAM
90FBGA**

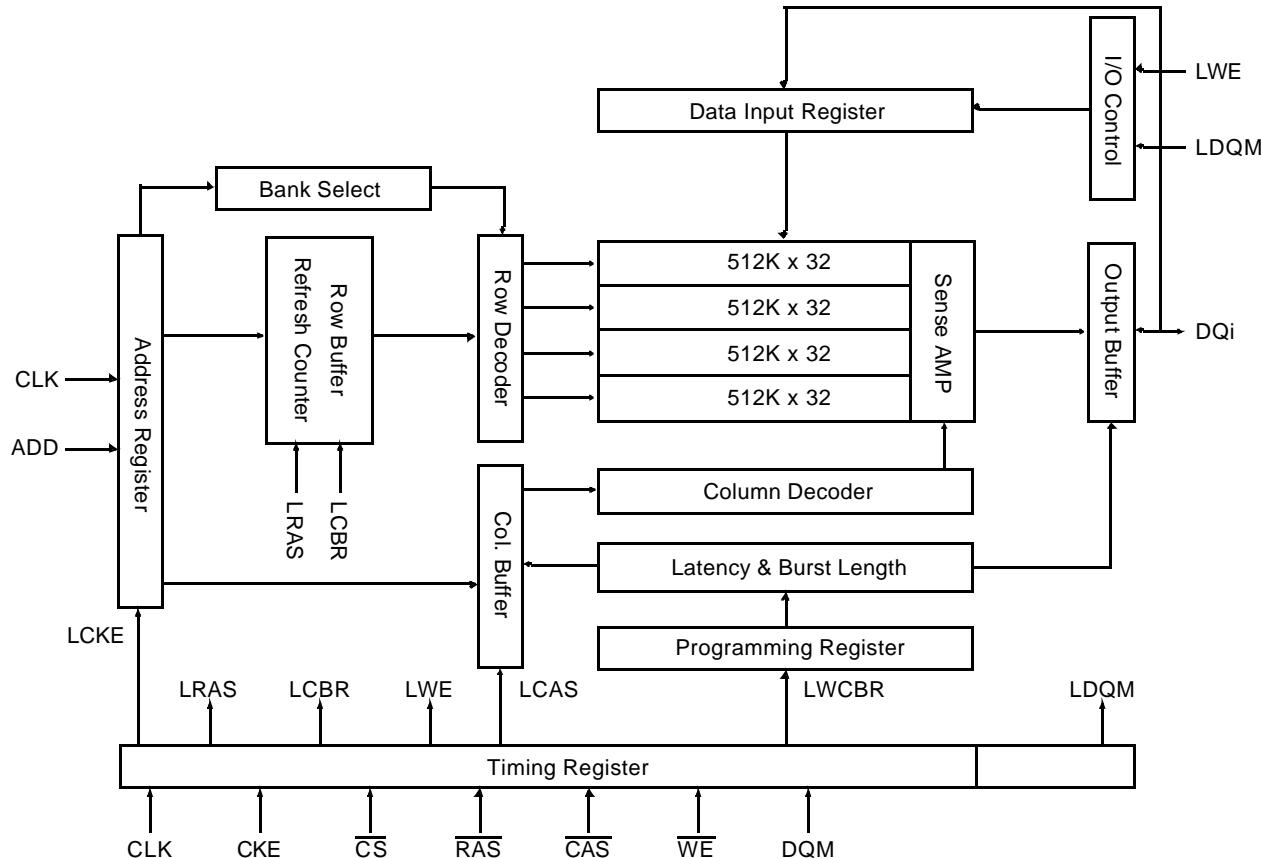
(VDD/VDDQ 2.5V/1.8V or 2.5V/2.5V, PASR & TCSR)

Revision 1.5

December 2002

512K x 32Bit x 4 Banks Mobile SDRAM**FEATURES**

- 2.5V Power Supply.
- LVC MOS compatible with multiplexed address.
- Four banks operation.
- MRS cycle with address key programs.
 - CAS latency (1 & 2 & 3).
 - Burst length (1, 2, 4, 8 & Full page).
 - Burst type (Sequential & Interleave).
- EMRS cycle with address key programs.
- All inputs are sampled at the positive going edge of the system clock .
- Burst read single-bit write operation.
- Special Function Support.
 - PASR (Partial Array Self Refresh).
 - TCSR (Temperature Compensated Self Refresh).
- DQM for masking.
- Auto & self refresh.
- 64ms refresh period (4K cycle).
- Extended temperature range : (-25°C to 85°C).
- 90balls FBGA(-SXXX -Pb, -DXXX -Pb Free).

FUNCTIONAL BLOCK DIAGRAM**GENERAL DESCRIPTION**

The K4S64323LF is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 524,288 words by 32 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst lengths and programmable latencies allow the same device to be useful for a variety of high bandwidth and high performance memory system applications.

ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
K4S64323LF-S(D)G/S75	133MHz(CL=3) ^{*1} 105MHz(CL=2)	LVC MOS	90FBGA Pb (Pb Free)
K4S64323LF-S(D)G/S1H	105MHz(CL=2)		
K4S64323LF-S(D)G/S1L	105MHz(CL=3) ^{*2}		
K4S64323LF-S(D)G/S15	66MHz(CL=2) ^{*3}		

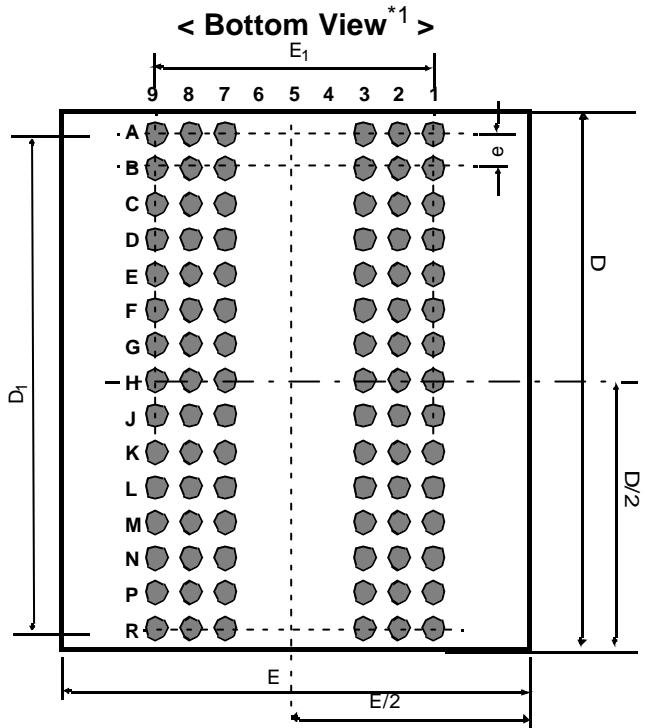
-S(D)S ; Super Low Power, Operating Temp : -25°C~85°C.

-S(D)G ; Low Power, Operating Temp : -25°C~85°C.

Notes :

1. In case of 55MHz Frequency, CL1 can be supported.
2. In case of 40MHz Frequency, CL1 can be supported.
3. In case of 33MHz Frequency, CL1 can be supported.

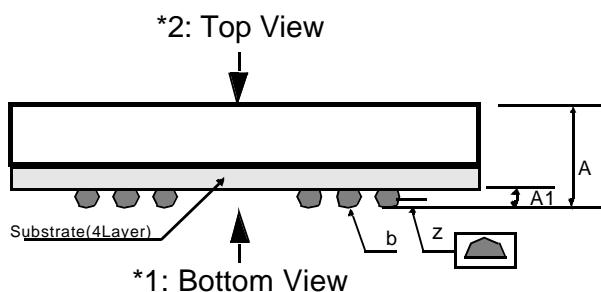
90-Ball FBGA Package Dimension and Pin Configuration



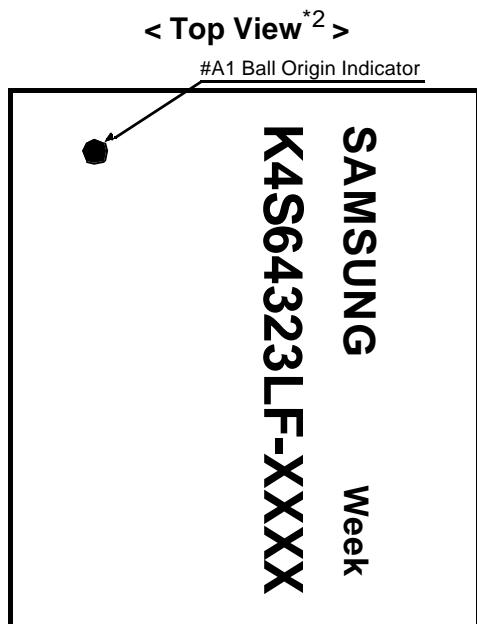
< Top View ^{*2} >

90Ball(6x15) CSP

	1	2	3	7	8	9
A	DQ26	DQ24	V _{SS}	V _{DD}	DQ23	DQ21
B	DQ28	V _{DDQ}	V _{SSQ}	V _{DDQ}	V _{SSQ}	DQ19
C	V _{SSQ}	DQ27	DQ25	DQ22	DQ20	V _{DDQ}
D	V _{SSQ}	DQ29	DQ30	DQ17	DQ18	V _{DDQ}
E	V _{DDQ}	DQ31	NC	NC	DQ16	V _{SSQ}
F	V _{SS}	DQM3	A3	A2	DQM2	V _{DD}
G	A4	A5	A6	A10	A0	A1
H	A7	A8	NC	NC	BA1	NC
J	CLK	CKE	A9	BA0	\overline{CS}	\overline{RAS}
K	DQM1	NC	NC	\overline{CAS}	\overline{WE}	DQM0
L	V _{DDQ}	DQ8	V _{SS}	V _{DD}	DQ7	V _{SSQ}
M	V _{SSQ}	DQ10	DQ9	DQ6	DQ5	V _{DDQ}
N	V _{SSQ}	DQ12	DQ14	DQ1	DQ3	V _{DDQ}
P	DQ11	V _{DDQ}	V _{SSQ}	V _{DDQ}	V _{SSQ}	DQ4
R	DQ13	DQ15	V _{SS}	V _{DD}	DQ0	DQ2



*1: Bottom View



Pin Name	Pin Function
CLK	System Clock
\overline{CS}	Chip Select
CKE	Clock Enable
A ₀ ~ A ₁₀	Address
B _{A0} ~ B _{A1}	Bank Select Address
\overline{RAS}	Row Address Strobe
\overline{CAS}	Column Address Strobe
\overline{WE}	Write Enable
DQM ₀ ~ DQM ₃	Data Input/Output Mask
DQ ₀ ~ 31	Data Input/Output
V _{DD} /V _{SS}	Power Supply/Ground
V _{DDQ} /V _{SSQ}	Data Output Power/Ground

[Unit:mm]

Symbol	Min	Typ	Max
A	-	1.30	1.40
A ₁	0.30	0.35	0.40
E	-	11.00	-
E ₁	-	6.40	-
D	-	13.00	-
D ₁	-	11.20	-
e	-	0.80	-
b	0.40	0.45	0.50
z	-	-	0.10

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 3.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 3.6	V
Storage temperature	T _{TSG}	-55 ~ +150	°C
Power dissipation	P _D	1	W
Short circuit current	I _{OS}	50	mA

Notes :

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = -25°C to 85°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	2.3	2.5	2.7	V	
	V _{DDQ}	1.65	-	2.7	V	
Input logic high voltage	V _{IH}	0.8 x V _{DDQ}	-	V _{DDQ} + 0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.3	V	2
Output logic high voltage	V _{OH}	V _{DDQ} -0.2V	-	-	V	I _{OH} = -0.1mA
Output logic low voltage	V _{OL}	-	-	0.2	V	I _{OL} = 0.1mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes:

1. V_{IH} (max) = 3.0V AC. The overshoot voltage duration is \leq 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is \leq 3ns.

3. Any input 0V \leq V_{IN} \leq V_{DDQ}.

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with tri-state outputs.

4. Dout is disabled, 0V \leq V_{OUT} \leq V_{DDQ}.

CAPACITANCE (V_{DD} = 2.5V, TA = 23°C, f = 1MHz, V_{REF} = 0.9V \pm 50 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	C _{CLK}	-	4.0	pF	
RAS, CAS, WE, CS, CKE, DQM ₀ ~ DQM ₃	C _{IN}	-	4.0	pF	
Address(A ₀ ~ A ₁₀ , BA ₀ ~ BA ₁)	C _{ADD}	-	4.0	pF	
DQ ₀ ~ DQ ₃₁	C _{OUT}	-	6.0	pF	

DC CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = -25°C to 85°C)

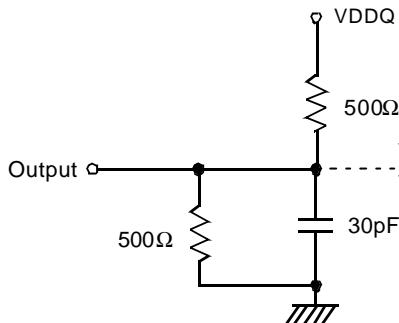
Parameter	Symbol	Test Condition	Version				Unit	Note				
			-75	-1H	-1L	-15						
Operating Current (One Bank Active)	Icc1	Burst length = 1 t _{RC} ≥ t _{RC(min)} I _O = 0 mA	70	70	65	60	mA	1				
Precharge Standby Current in power-down mode	Icc2P	CKE ≤ V _{IL(max)} , t _{CC} = 10ns	0.5				mA					
	Icc2PS	CKE & CLK ≤ V _{IL(max)} , t _{CC} = ∞	0.5									
Precharge Standby Current in non power-down mode	Icc2N	CKE ≥ V _{IH(min)} , CS ≥ V _{IH(min)} , t _{CC} = 10ns Input signals are changed one time during 20ns	10				mA					
	Icc2NS	CKE ≥ V _{IH(min)} , CLK ≤ V _{IL(max)} , t _{CC} = ∞ Input signals are stable	7									
Active Standby Current in power-down mode	Icc3P	CKE ≤ V _{IL(max)} , t _{CC} = 10ns	5				mA					
	Icc3PS	CKE & CLK ≤ V _{IL(max)} , t _{CC} = ∞	5									
Active Standby Current in non power-down mode (One Bank Active)	Icc3N	CKE ≥ V _{IH(min)} , CS ≥ V _{IH(min)} , t _{CC} = 10ns Input signals are changed one time during 20ns	20				mA					
	Icc3NS	CKE ≥ V _{IH(min)} , CLK ≤ V _{IL(max)} , t _{CC} = ∞ Input signals are stable	20				mA					
Operating Current	Icc4	I _O = 0 mA, Page burst	85	70	70	60	mA	1				
Refresh Current	Icc5	t _{RC} ≥ t _{RC(min)}	115	110	100	80	mA	2				
Self Refresh Current	Icc6	CKE ≤ 0.2V	TCSR Range		Max 45°C		Max 85°C		°C			
			-S(D)G	4 Banks	235		350		uA	3		
				2 Banks	210		290					
				1 Bank	195		270					
			-S(D)S	4 Banks	130		230		uA	4		
				2 Banks	105		170					
				1 Bank	90		150					

Notes :

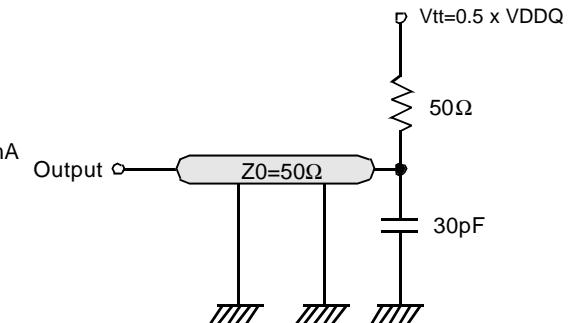
1. Measured with outputs open.
2. Refresh period is 64ms.
3. K4S64323LF-S(D)G**
4. K4S64323LF-S(D)S**
5. Unless otherwise noted, input swing level is CMOS(V_{IH} / V_{IL}=V_{DDQ}/V_{SSQ}).

AC OPERATING TEST CONDITIONS ($V_{DD} = 2.5V \pm 0.2V$, $T_A = -25^\circ C$ to $85^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	$0.9 \times V_{DDQ} / 0.2$	V
Input timing measurement reference level	$0.5 \times V_{DDQ}$	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	$0.5 \times V_{DDQ}$	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version				Unit	Note		
		-75	-1H	-1L	-15				
Row active to row active delay	$t_{RRD}(\text{min})$	15	19	19	30	ns	1		
RAS to CAS delay	$t_{RC}(\text{min})$	19	19	24	30	ns	1		
Row precharge time	$t_{RP}(\text{min})$	19	19	24	30	ns	1		
Row active time	$t_{RAS}(\text{min})$	45	50	60	60	ns	1		
	$t_{RAS}(\text{max})$	100				us			
Row cycle time	$t_{RC}(\text{min})$	65	70	84	90	ns	1		
Last data in to row precharge	$t_{RDL}(\text{min})$	2				CLK	2,3		
Last data in to Active delay	$t_{DAL}(\text{min})$	$t_{RDL} + t_{RP}$				-	3		
Last data in to new col. address delay	$t_{CDL}(\text{min})$	1				CLK	2		
Last data in to burst stop	$t_{BDL}(\text{min})$	1				CLK	2		
Col. address to col. address delay	$t_{CCD}(\text{min})$	1				CLK	4		
Number of valid output data	CAS latency=3	2				ea	5		
	CAS latency=2	1							
	CAS latency=1	-							

Notes :

- The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
- Minimum delay is required to complete write.
- Minimum $t_{RDL}=2\text{CLK}$ and $t_{DAL}(=t_{RDL} + t_{RP})$ is required to complete both of last data write command(t_{RDL}) and precharge command(t_{RP}). $t_{RDL}=1\text{CLK}$ can be supported only in the case under 100MHz with manual precharge mode.
- All parts allow every cycle column address change.
- In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS(AC operating conditions unless otherwise noted)

Parameter		Symbol	- 75		-1H		-1L		- 15		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tcc	7.5	1000	9.5	1000	9.5	1000	15	1000	ns	1
	CAS latency=2		9.5		9.5		12		15			
	CAS latency=1		-		-		25		30			
CLK to valid output delay	CAS latency=3	tsac		5.4		7		7		9	ns	1,2
	CAS latency=2			7		7		8		9		
	CAS latency=1			-		-		20		24		
Output data hold time	CAS latency=3	toH	2.5		2.5		2.5		2.5		ns	2
	CAS latency=2		2.5		2.5		2.5		2.5			
	CAS latency=1		-		-		2.5		2.5			
CLK high pulse width		tch	2.5		3		3		3.5		ns	3
CLK low pulse width		tcl	2.5		3		3		3.5		ns	3
Input setup time		tss	2.0		2.5		2.5		3.5		ns	3
Input hold time		tsh	1.0		1.5		1.5		2.0		ns	3
CLK to output in Low-Z		tslz	1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tshz		5.4		7		7		9	ns	
	CAS latency=2			7		7		8		9		
	CAS latency=1			-		-		20		24		

Notes :

1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.

If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

Note :

1. Samsung are not designed or manufactured for use in a device or system that is used under circumstance in which human life is potentially at stake. Please contact to the memory marketing team in samsung electronics when considering the use of a product contained herein for any specific purpose, such as medical, aerospace, nuclear, military, vehicular or undersea repeater use.

SIMPLIFIED TRUTH TABLE (V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND		CKEn-1	CKEn	CS	RAS	CAS	WE	DQM	BA _{0,1}	A _{10/AP}	A _{9~A₀}	Note				
Register	Mode Register Set	H	X	L	L	L	L	X	OP CODE			1, 2				
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3			
	Self Refresh			L						X			3			
	Exit	L	H	L	H	H	H	X	X			3				
				Bank Active & Row Addr.				H	X	L	L	H	H	X	V	Row Address
Read & Column Address		Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A _{0~A₇})	4		
		Auto Precharge Enable												4, 5		
Write & Column Address		Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A _{0~A₇})	4		
		Auto Precharge Enable												4, 5		
Burst Stop			H	X	L	H	H	L	X	X				6		
Precharge		Bank Selection		H	X	L	L	H	L	X	V	L	X			
		All Banks														
Clock Suspend or Active Power Down	Entry	H	L	H	X	X	X	X	X							
				L	V	V	V		X							
Precharge Power Down Mode	Exit	L	H	X	X	X	X	X	X							
				H	X	X	X		X							
DQM			H	X				V	X				7			
No Operation Command			H	X	H	X	X	X	X	X						
				L	H	H	H									

Notes :

1. OP Code : Operand Code

A₀ ~ A₁₀ & BA₀ ~ BA₁ : Program keys. (@MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are the same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA₀ ~ BA₁ : Bank select addresses.If both BA₀ and BA₁ are "Low" at read, write, row active and precharge, bank A is selected.If BA₀ is "Low" and BA₁ is "High" at read, write, row active and precharge, bank B is selected.If BA₀ is "High" and BA₁ is "Low" at read, write, row active and precharge, bank C is selected.If both BA₀ and BA₁ are "High" at read, write, row active and precharge, bank D is selected.If A_{10/AP} is "High" at row precharge, BA₀ and BA₁ are ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at the positive going edge of CLK masks the data-in at that same CLK in write operation (Write DQM latency is 0), but in read operation it makes the data-out Hi-Z state after 2 CLK cycles. (Read DQM latency is 2).